AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for developing and verifying a FPGA-based SoC, the method comprising:

executing software code for a logic analyzer located within the FPGA-based SoC, said software code being the core software code for said logic analyzer;

defining at least one monitor probe point within the FPGA-based SoC for analysis by said logic analyzer, wherein the software code includes at least one trigger subject to control by a processor included within said FPGA-based SoC for ~~and~~ the at least one monitor probe point ~~defined are created~~ during customization of said FPGA-based SoC; and

collecting information for said at least one monitor probe point to facilitate analysis of signals while developing and verifying the FPGA-based SoC.

2. (Original) The method according to claim 1, wherein said collecting step further comprises the step of capturing electronic signal data for said monitor probe point.

3. (Original) The method according to claim 2, wherein said capturing step further comprises the step of capturing trace information for said monitor probe point.

4. (Original) The method according to claim 2, wherein said capturing step further comprises the step of establishing triggers for causing the collection of trigger information for said monitor probe point.

5. (Original) The method according to claim 1, further comprising the step of receiving said collected information for said monitor probe point by an external monitor tool comprising an interface for communicating with said logic analyzer located within the FPGA-based SoC.

6. (Original) The method according to claim 5, further comprising the step of translating said collected information into a waveform representing trigger and trace capture.

7. (Original) The method according to claim 6, wherein said translating step further comprises the step of displaying said waveform of said trigger and said trace capture on a display for said monitoring tool.

8. (Original) The method according to claim 1, wherein said monitor probe point is selected from the group consisting of an internal node of the FPGA-based SoC, a device pin and/or a data bus line of the FPGA-based SoC.

9. (Original) The method according to claim 1, further comprising the step of integrating said software code for said logic analyzer within said FPGA-based SoC.

10. (Original) The method according to claim 1, further comprising the step of downloading said software code for said logic analyzer to said FPGA-based SoC.

11. (Currently Amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine to perform the steps of:

executing software code for a logic analyzer located within an FPGA-based SoC, said software code being the core software code for said logic analyzer utilized for developing and verifying said FPGA-based SoC;

defining at least one monitor probe point and at least one trigger for ~~within~~ said FPGA-based SoC for analysis by said logic analyzer, said FPGA-based SoC including a processor, wherein ~~the software code and at least one monitor probe point~~ said at least one trigger ~~defined are created~~ is monitored with said logic analyzer and subject to control by said processor for

acquisition of trigger information during customization of said FPGA-based SoC; and

collecting information for said at least one monitor probe point to facilitate analysis of signals while developing and verifying said FPGA-based SoC.

12. (Original) The machine readable storage according to claim 11, wherein said collecting step further comprises the step of capturing electronic signal data for said monitor probe point.

13. (Original) The machine readable storage according to claim 12, wherein said capturing step further comprises the step of capturing trace information for said monitor probe point.

14. (Original) The machine readable storage readable storage according to claim 12, wherein said capturing step further comprises the step of establishing triggers for causing the collection of trigger information for said monitor probe point.

15. (Original) The machine readable storage according to claim 11, further comprising the step of receiving said collected information for said monitor probe point by an external monitor tool comprising an interface for communicating with said logic analyzer located within said FPGA-based SoC.

16. (Original) The machine readable storage according to claim 15, further comprising the step of translating said collected information into a waveform representing trigger and trace capture.

17. (Original) The machine readable storage according to claim 16, wherein said translating step further comprises the step of displaying said waveform of said trigger and said trace capture on a display for said monitoring tool.

18. (Original) The machine readable storage according to claim 11, wherein said monitor probe point is selected from the group consisting of an internal node of said FPGA-based SoC, a device pin and/or a data bus line of said FPGA-based embedded processor SoC.

19. (Original) The machine readable storage according to claim 11, further comprising the step of integrating said software code for said logic analyzer within said FPGA-based SoC.

20. (Original) The machine readable storage according to claim 11, further comprising the step of downloading said software code for said logic analyzer to said FPGA-based SoC.

21. (Currently Amended) A FPGA-based SoC development and verification system, the system comprising:

a software core for a logic analyzer inserted within ~~the~~ an FPGA-based SoC during customization of the FPGA-based SoC, the FPGA-based SoC including a processor for carrying out instruction of the software core for control of one or more triggers;

an external software monitor tool having an interface for communicating with said logic analyzer software core; and

a communication port for facilitating exchange of data between said logic analyzer software core and said external monitor tool.

22. (Original) The FPGA-based SoC development and verification system according to claim 21, further comprising a controller integrated within the FPGA-based SoC for facilitating the communication of information between said logic analyzer software core and said communication port.

23. (Original) The FPGA-based SoC development and verification system according to claim 21, wherein said external software monitor tool further comprises a graphical user interface (GUI)

for selecting and modifying trigger and setup functions and for displaying waveforms for trace and captured information.

Claim 24 (Cancelled).

25. (Currently Amended) A GUI for development and verification of a FPGA-based SoC, the GUI comprising:

a selection dialog for defining and selecting monitor probe points and for defining triggers subject to control by a processor of the FPGA-based SoC;

a display window for displaying waveforms for trace and trigger conditions; and

a communication interface for facilitating communication with a logic analyzer core integrated within the FPGA-based SoC.

26. (Original) The GUI according to claim 25, wherein said selection dialog further comprises an object for establishing a trigger condition.

27. (Original) The GUI according to claim 25, wherein said selection dialog further comprises contains objects for establishing trace parameters for said monitor probe points.

28. (Original) The GUI according to claim 25, wherein said selection dialog presents a selection attribute selected from the group consisting of target device family, clock edge, trigger type, trigger match unit type, number of trigger match units, data depth, data width, and trigger width.

29. (Currently Amended) A method for developing and verifying a FPGA-based SoC within a system, the method comprising:

executing software code for a logic analyzer located within the FPGA-based SoC, the software code being the core software code for the logic analyzer;

defining at least one monitor probe point and at least one trigger for ~~within~~ the FPGA-based SoC for analysis by the logic

analyzer, wherein the software code, ~~and~~ the at least one monitor probe point, and the at least one trigger defined are created during customization of the FPGA-based SoC, the at least one trigger subject to control by a processor of the FPGA-based SoC; and

collecting information for the at least one monitor probe point to facilitate analysis of signals within the system while developing and verifying the FPGA-based SoC.

Claims 30-31 (Cancelled)

32. (Currently Amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections, the code sections executable by a machine for causing the machine to perform the steps of:

executing software code for a logic analyzer located within an FPGA-based SoC portion of a system, the software code being the core software code for the logic analyzer utilized for developing and verifying the FPGA-based SoC;

defining at least one monitor probe point and at least one trigger for ~~within~~ the FPGA-based SoC for analysis by the logic analyzer, wherein the software code, ~~and~~ the at least one monitor probe point, and the at least one trigger defined are created during customization of the FPGA-based SoC, the at least one trigger subject to control by a processor of the FPGA-based SoC; and

collecting information for the at least one monitor probe point to facilitate analysis of signals within the system while developing and verifying the FPGA-based SoC.

Claims 33-34 (Cancelled)

35. (Currently Amended) A GUI for development and verification of a system including an FPGA-based SoC, the GUI comprising:

a selection dialog for defining and selecting monitor probe points and at least one trigger for ~~within~~ the system, the

monitor probe points being located within the FPGA-based SoC, the at least one trigger subject to control by a processor of the FPGA-based SoC;

a display window for displaying waveforms for trace and trigger conditions; and

a communication interface for facilitating communication with a logic analyzer core integrated within the FPGA-based SoC.

Claims 36-37 (Cancelled)